



## Modulelink(Shenzhen) Technology Co.,Ltd.

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### 40Gb/s CFP ER4 Optical Transceiver MCFP-40G-LR4

#### **Features**

- 4x10Gb/s parallel optical interface compliant to 802.3ba 40G LR4
- Uncooled 4 CWDM DFB transmitters and PIN photodiode receivers
- Form factors compliant to CFP MSA
- XLAUI High Speed Electrical Interface
- IEEE compliant MDIO interface for management and digital diagnostic monitor
- Single +3.3V power supply, operating case temperature: 0~70C
- All-metal housing for superior EMI performance
- Advanced firmware allows encryption information of customer system stored in transceiver

#### **Applications**

- Rack to rack
- Data centers
- Metro networks
- Switches and Routers

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### 1. General Description

The MCFP-40G-LR4 is a 40Gb/s transceiver module for optical communication applications compliant to 40GBASE-LR4 of the IEEE P802.3ba standard. The module converts 4 inputs channels of 10Gb/s electrical data to 4 CWDM optical signals and then multiplexes them into a single channel for 40Gb/s optical transmission. Reversely on the receiver side, the module de-multiplexes a 40Gb/s optical input into 4 CWDM channels of optical signals and then converts them to electrical data for 4 output channels.

The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm as members of the CWDM wavelength grid defined in ITU-T G694.2. For SMF applications, the transceiver module has an operating range of 2m~10km.

The MCFP-40G-LR4 is designed with form factor, optical/electrical connection and MDIO interface according to the CFP Multi-Source Agreement (MSA). The innovative design has all the fibers inside the CFP package configured without any splicing or non-permanent connector. Also, fiber routines are neatly organized and fixed inside a SUS304 container. For mechanical and environmental reliability, the WDM sections are aligned and secured to the container by laser welder, and then aligned and affixed with each CWDM laser or PIN/TIA TO to form an integrated structure of TOSA or ROSA.

### 2. Functional Description

The MCFP-40G-LR4 contains a duplex SC connector for the optical interface and a 148-pin connector for the electrical interface. The chart in section 3 shows the functional block diagram of the MCFP-40G-LR4 CFP Transceiver.

#### Transmitter Operation

The transceiver module receives 4 channels of 10Gb/s electrical data, which are processed by a 4 channel Clock Data Recovery (CDR) IC that reshapes and reduces the jitter of each electrical signal. Subsequently, a DML laser driver IC converts each channel of the 4 electrical signals to optical signal from one of the 4 CWDM lasers. The optical output power is maintained constant by an automatic power control (APC) circuit. All of 4 optical signals are multiplexed by CWDM filters in a daisy-chain configuration to form a single optical output of 40Gb/s.

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### Receiver Operation

The receiver section de-multiplexes the optical input of 40Gb/s signal into 4 optical signals of CWDM wavelengths. Each optical signal is converted to electrical signal by one of 4 PIN/TIA. All of the 4 electrical signals are feed to another CDR IC that provides limiting amplification, and reshapes and retimes each electrical signal as one of the 4 output channels.

### MDIO Interface

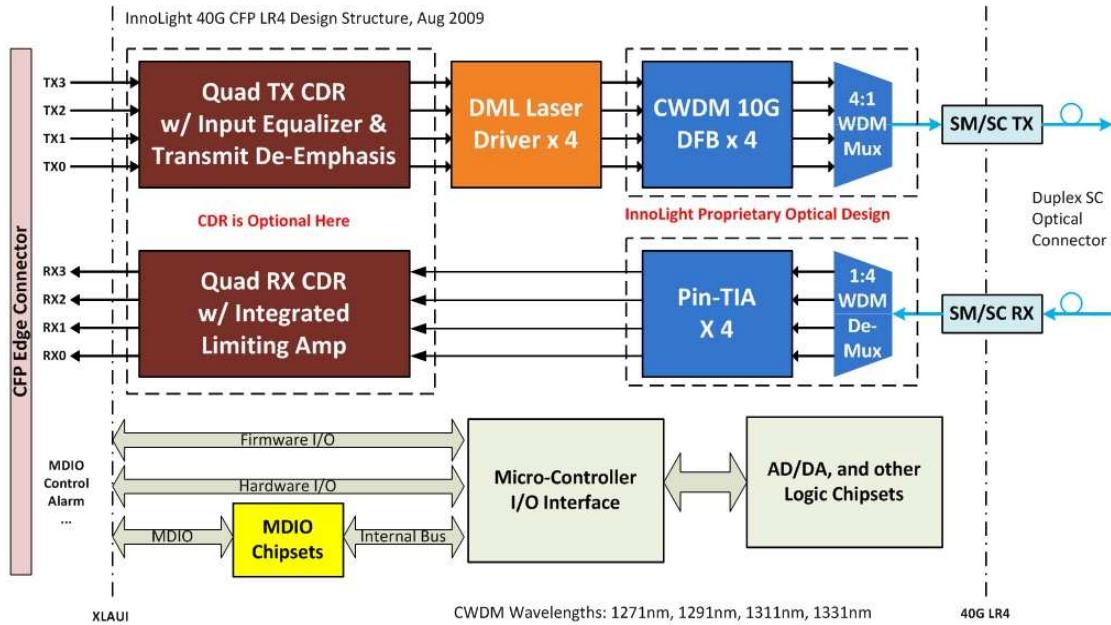
The CFP Module supports alarm, control and monitor functions via hardware pins and via an MDIO bus. Upon module initialization, these functions are available.

CFP MDIO electrical interface consists of 8 wires including 2 wires of MDC and MDIO, as well as 5 Port Address wires, and the Global Alarm wire. MDC is the MDIO Clock line driven by host and MDIO is the bidirectional data line driven by both host and module depending upon the data directions. The CFP uses pins in the electrical connector to instantiate the MDIO interface, listed in Table 2-4: MDIO Interface Pins.

Pin #	Symbol	Description	I/O	Logic	"H"	"L"
41	GLB_ALRMn	Global Alarm	O	3.3V LVCMOS	OK	Alarm
47	MDIO	Management Data Input Output Bi-Directional Data	I/O	1.2V LVCMOS		
48	MDC	MDIO Clock	I	1.2V LVCMOS		
46	PRTADR0	MDIO port address bit 0	I	1.2V LVCMOS	per MDIO document	
45	PRTADR1	MDIO port address bit 1	I	1.2V LVCMOS		
44	PRTADR2	MDIO port address bit 2	I	1.2V LVCMOS		
43	PRTADR3	MDIO port address bit 3	I	1.2V LVCMOS		
42	PRTADR4	MDIO port address bit 4	I	1.2V LVCMOS		

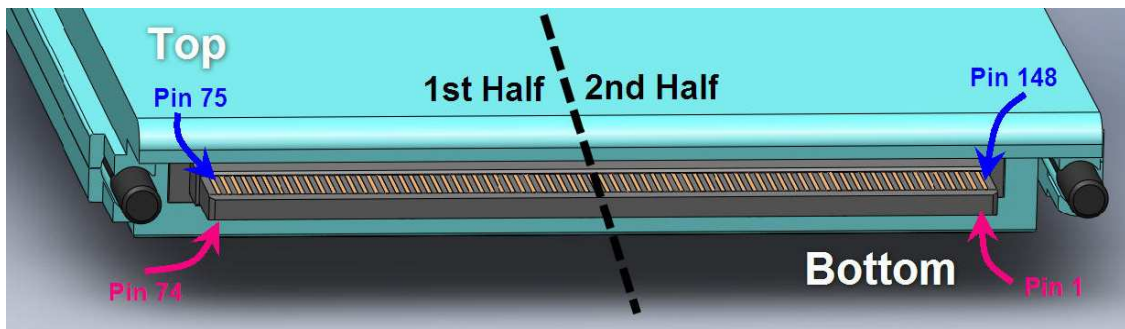
### Transceiver Block Diagram

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**Pin Assignment and Pin Description**

The CFP connector has 148 pins which are arranged in Top and Bottom rows. The pin map is shown in Table 5-4 below. The detailed description of the Bottom row ranges from pin 1 through pin 74 and is shown in Table 5-5 below. The pin orientation is shown below in Figure 5-26.



**CFP Transceiver Electrical Pad Layout**

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	Top Row (2nd Half)		Bottom Row (2nd Half)		Top Row (1st Half)		Bottom Row (1st Half)
148	GND	1	3.3V_GND	111	GND	38	MOD_ABS
147	REFCLKn	2	3.3V_GND	110	(RX_DSCn)	39	MOD_RSTn
146	REFCLKp	3	3.3V_GND	109	(RX_DSCp)	40	RX_LOS
145	GND	4	3.3V_GND	108	GND	41	GLB_ALRMn
144	(TX_DSCn)	5	3.3V_GND	107	RX9n	42	PRTADR4
143	(TX_DSCp)	6	3.3V	106	RX9p	43	PRTADR3
142	GND	7	3.3V	105	GND	44	PRTADR2
141	TX9n	8	3.3V	104	RX8n	45	PRTADR1
140	TX9p	9	3.3V	103	RX8p	46	PRTADR0
139	GND	10	3.3V	102	GND	47	MDIO
138	TX8n	11	3.3V	101	RX7n	48	MDC
137	TX8p	12	3.3V	100	RX7p	49	GND
136	GND	13	3.3V	99	GND	50	VND_IO_F
135	TX7n	14	3.3V	98	RX6n	51	VND_IO_G
134	TX7p	15	3.3V	97	RX6p	52	GND
133	GND	16	3.3V_GND	96	GND	53	VND_IO_H
132	TX6n	17	3.3V_GND	95	RX5n	54	VND_IO_J
131	TX6p	18	3.3V_GND	94	RX5p	55	3.3V_GND
130	GND	19	3.3V_GND	93	GND	56	3.3V_GND
129	TX5n	20	3.3V_GND	92	RX4n	57	3.3V_GND
128	TX5p	21	VND_IO_A	91	RX4p	58	3.3V_GND
127	GND	22	VND_IO_B	90	GND	59	3.3V_GND
126	TX4n	23	GND	89	RX3n	60	3.3V
125	TX4p	24	(TX_MCLKn)	88	RX3p	61	3.3V
124	GND	25	(TX_MCLKp)	87	GND	62	3.3V
123	TX3n	26	GND	86	RX2n	63	3.3V
122	TX3p	27	VND_IO_C	85	RX2p	64	3.3V
121	GND	28	VND_IO_D	84	GND	65	3.3V
120	TX2n	29	VND_IO_E	83	RX1n	66	3.3V
119	TX2p	30	PRG_CNTL1	82	RX1p	67	3.3V
118	GND	31	PRG_CNTL2	81	GND	68	3.3V
117	TX1n	32	PRG_CNTL3	80	RX0n	69	3.3V
116	TX1p	33	PRG_ALRM1	79	RX0p	70	3.3V_GND
115	GND	34	PRG_ALRM2	78	GND	71	3.3V_GND
114	TX0n	35	PRG_ALRM3	77	(RX_MCLKn)	72	3.3V_GND
113	TX0p	36	TX_DIS	76	(RX_MCLKp)	73	3.3V_GND
112	GND	37	MOD_LOPWR	75	GND	74	3.3V_GND

Bottom side Pin Definitions.

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PIN #	NAME	I/O	Logic	Description
1	3.3V_GND			3.3V Module Supply Voltage Return Ground,can be separte or tied together with Signal Ground
2	3.3V_GND			
3	3.3V_GND			
4	3.3V_GND			
5	3.3V_GND			
6	3.3V			3.3V Module Supply Voltage
7	3.3V			
8	3.3V			
9	3.3V			
10	3.3V			
11	3.3V			
12	3.3V			
13	3.3V			
14	3.3V			
15	3.3V			
16	3.3V_GND			3.3V Module Supply Voltage Return Ground,can be separte or tied together with Signal Ground
17	3.3V_GND			
18	3.3V_GND			
19	3.3V_GND			
20	3.3V_GND			
21	VND_IO_A	I/O		Moudle Vendor I/O A.Do Not Connect!
22	VND_IO_B	I/O		Moudle Vendor I/O B.Do Not Connect!
23	GND			
24	(TX_MCLK <sub>n</sub> )	O	CML	For optical waveform testing.Not for normal use.
25	(TX_MCLK <sub>p</sub> )	O	CML	For optical waveform testing.Not for normal use.
26	GND			

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27	VND_IO_C	I/O		Moudle Vendor I/O C.Do Not Connect!
28	VND_IO_D	I/O		Moudle Vendor I/O D.Do Not Connect!
29	VND_IO_E	I/O		Moudle Vendor I/O E.Do Not Connect!
30	PRG_CNTL1	I	LVC MOS w/ PUR	Programmable Control 1 set over MDIO, MSA Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1" or NC: enabled = not used
31	PRG_CNTL2	I	LVC MOS w/ PUR	Programmable Control 2 set over MDIO, MSA Default: Hardware Interlock LSB, "00": <8W, "01": <16W, "10": <24W, "11" or NC: >24W = not used
32	PRG_CNTL3	I	LVC MOS w/ PUR	Programmable Control 3 set over MDIO, MSA Default: Hardware Interlock MSB, "00": <8W, "01": <16W, "10": <24W, "11" or NC: >24W = not used
33	PRG_ALARM1	O	LVC MOS	Programmable Alarm 1 set over MDIO, MSA Default: RXS, RX CDR Lock Indicator, "1": loss of lock, "0": locked
34	PRG_ALARM2	O	LVC MOS	Programmable Alarm 2 set over MDIO, MSA Default: HIPWR_ON, "1": module power up completed, "0": module not powered up
35	PRG_ALARM3	O	LVC MOS	Programmable Alarm 3 set over MDIO, MSA Default: MOD_READY, initialization sequence done, "1": done, "0": not done
36	TX_DIS	I	LVC MOS w/ PUR	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled
37	MOD_LOPWR	I	LVC MOS w/ PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled

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38	MOD_ABS	O	GND	Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host
39	MOD_RSTn	I	LVC MOS w/ PDR	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module
40	RX_LOS	O	LVC MOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition
41	GLB_ALRMn	O	LVC MOS	Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition
42	PRTADR4	I	1.2V CMOS	MDIO port address bit 4
43	PRTADR3	I	1.2V CMOS	MDIO port address bit 3
44	PRTADR2	I	1.2V CMOS	MDIO port address bit 2
45	PRTADR1	I	1.2V CMOS	MDIO port address bit 1
46	PRTADR0	I	1.2V CMOS	MDIO port address bit 0
47	MDIO	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per 802.3ae and ba)
48	MDC	I	1.2V CMOS	Management Data Clock (electrical specs as per 802.3ae and ba)
49	GND			
50	VND_IO_F	I/O		Module Vendor I/O F. Do Not Connect!
51	VND_IO_G	I/O		Module Vendor I/O G. Do Not Connect!
52	GND			
53	VND_IO_H	I/O		Module Vendor I/O H. Do Not Connect!
54	VND_IO_J	I/O		Module Vendor I/O J. Do Not Connect!
55	3.3V_GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
56	3.3V_GND			
57	3.3V_GND			

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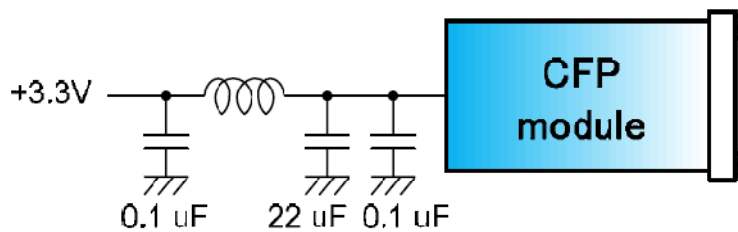


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58	3.3V_GND			
59	3.3V_GND			
60	3.3V			3.3V Module Supply Voltage
61	3.3V			
62	3.3V			
63	3.3V			
64	3.3V			
65	3.3V			
66	3.3V			
67	3.3V			
68	3.3V			
69	3.3V			
70	3.3V_GND			3.3V Module Supply Voltage Return Ground,can be separte or tied together with Signal Ground
71	3.3V_GND			
72	3.3V_GND			
73	3.3V_GND			
74	3.3V_GND			

**Recommended Power Supply Filter**



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### 3. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	Tst	-40	85	degC	
Relative Humidity (non-condensation)	RH	-	85	%	
Operating Case Temperature	Topc	0	70	degC	1
Supply Voltage	VCC3	-0.5	3.6	V	
Voltage on LVTTL Input	Vilvttl	-0.5	VCC3+0.5	V	
LVTTL Output Current	Iolvttl	-	15	mA	
Voltage on Open Collector Output	Voco	0	6	V	
Receiver Input Optical Power(Average)	Mip	-	3	dBm	2

#### Notes:

1. Ta: -10 to 60degC with 1.5m/s airflow with an additional heat sink.
2. Pin Receiver.

### 4. Recommended Operating Conditions and Supply Requirements

Parameter	Symbol	Min	Max	Unit
Operating Case Temperature	Topc	0	70	degC
Relative Humidity (non-condensing)	Rhop	-	85	%
Power Supply Voltage	VCC3	3.135	3.465	V
Power Supply Current	ICC3	-	2500	mA
Total Power Consumption	Pd	-	6	W

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### 5. Optical Interface

<b>Transmitter Optical Interface</b>						
Parameter	Symbol	Min	Typical	Max	Unit	Note
Operating Data Rate	-	9.95		10.70	Gb/s	1
Output Center Wavelength	l <sub>tc</sub>	1264.5 to 1277.5 1284.5 to 1297.5 1304.5 to 1317.5 1324.5 to 1337.5			nm	
Spectral Width	d <sub>l</sub>	-		1	nm	
SMSR	SMSR	30		-	dB	
Average Output Power	P <sub>o</sub>	-6		1	dBm	2
Disabled Power	P <sub>off</sub>	-		-30	dBm	2
Extinction Ratio	ER	3.5		-	dB	2
Minimum OMA-TDP (10G Ethernet)	OMAt <sub>dp</sub>	-5.2		-	dBm	3
Eye Mask 2 (10G Ethernet)		IEEE802.3ae				3
Generation Jitter 1 (20kHz - 80MHz)		-		0.15	Ulp-p	2,4
Generation Jitter 2 (4MHz - 80MHz)		-		0.1	Ulp-p	2,4
RIN	RIN	-		-128	dB/Hz	
<b>Optical Path</b>						
Parameter	Symbol	Min	Typical	Max	Unit	Note
Operating Distance (10G Ethernet)		-		10	km	
Channel Insertion Loss (10G Ethernet)		0		6	dB	

<b>Receiver Optical Interface</b>						
Parameter	Symbol	Min	Typical	Max	Unit	Note
Operating Data Rate	-	9.95		10.70	Gb/s	1

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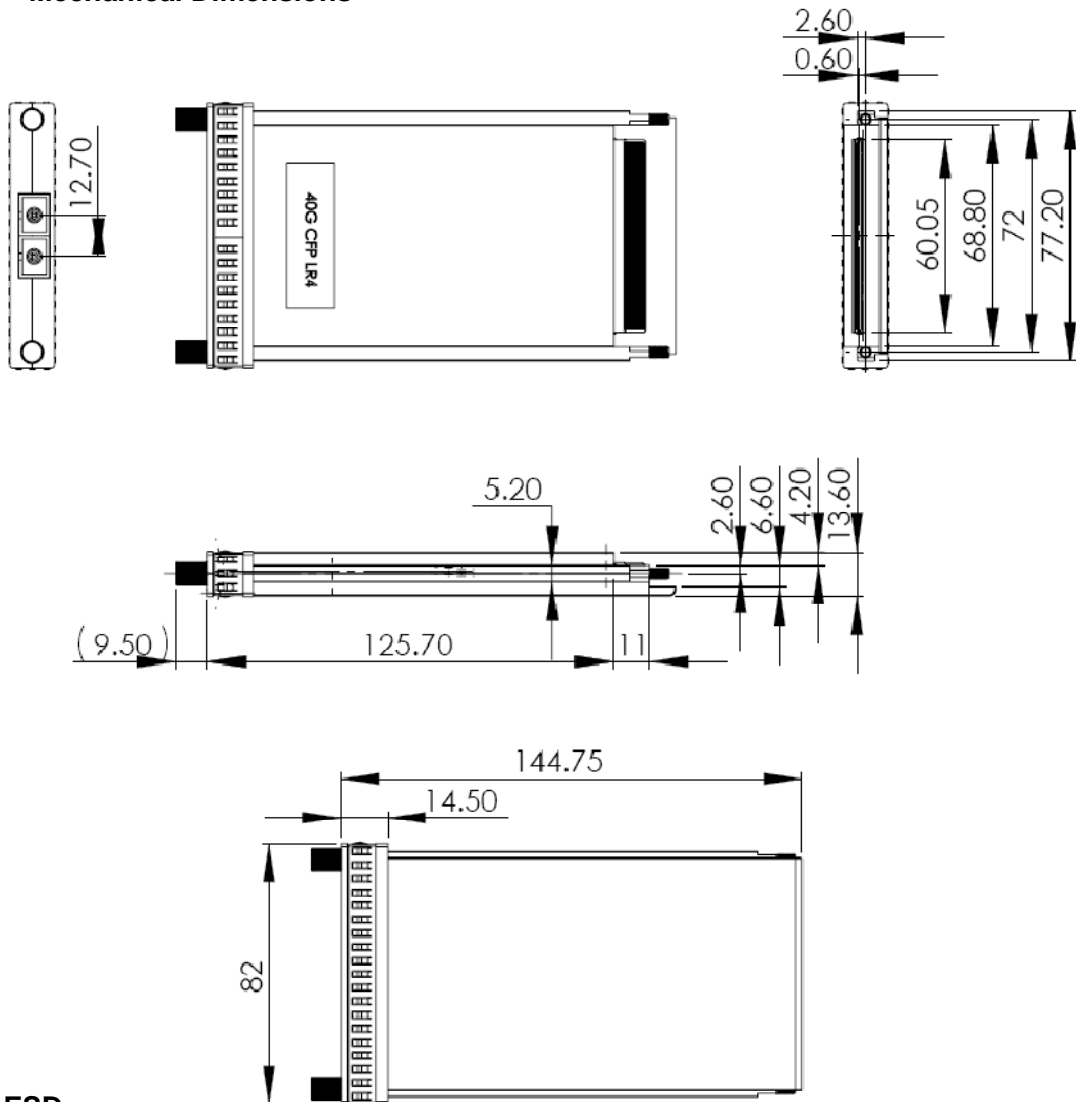
Input Center Wavelength	Irc	1264.5 to 1277.5 1284.5 to 1297.5 1304.5 to 1317.5 1324.5 to 1337.5			nm	
Overload	Rovl	0.5		-	dBm	
Minimum Sensitivity	Pmin	-	-18	-14.6	dBm	2
Sensitivity in OMA	OMA0	-		-12.6	dBm	3
Stressed Sensitivity in OMA	OMAst	-		-10.3	dBm	3
RX_LOS Assert Level	RLOSa	-25			dBm	
RX_LOS Deassert Level	RLOSd			-15	dBm	
RX_LOS Hysteresis	RLOSh	1		5	dB	
Optical Path Penalty	PN	-		1	dB	1
Optical Return Loss	ORL	14		-	dB	
Jitter Tolerance	JTL	GR-253-CORE/ITU-T G.783				

### Notes:

1. Data rate tolerance
  - 10GBASE-LR/LW: typ.+/-100ppm
2. Measured at 10.3125Gbps,Non-framed PRBS2^31-1,NRZ
3. Measured by using Modulelink XFP evaluation board.

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**6. Mechanical Dimensions**



**8. ESD**

This transceiver is specified as ESD threshold 2kV for all electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

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### 9. Laser Safety

This is a Class 1 Laser Product according to IEC 60825-1:1993:+A1:1997+A2:2001. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (July 26, 2007)

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